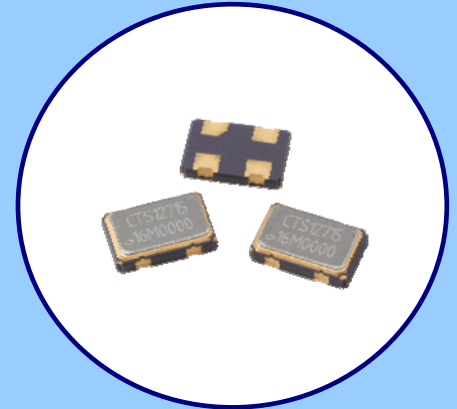


FEATURES

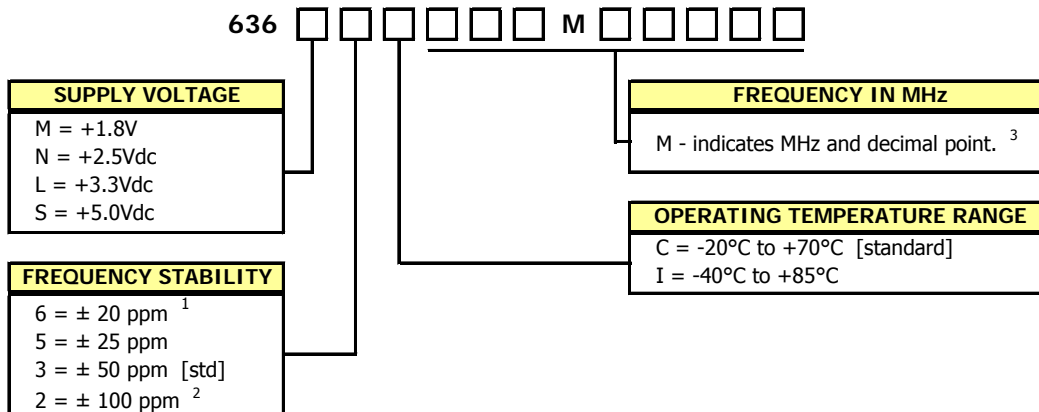
- Standard 5.0mm x 3.2mm 4-Pad Surface Mount Package
- HCMOS/TTL Compatible Output
- Fundamental and 3rd Overtone Crystal Designs
- Frequency Range 1 – 160 MHz
- Frequency Stability ± 50 ppm Standard, ± 25 ppm and ± 20 ppm Available
- Operating Voltages +1.8Vdc, +2.5Vdc, +3.3Vdc or +5.0Vdc
- Operating Temperature to -40°C to +85°C
- Output Enable Standard
- Tape & Reel Packaging Standard, EIA-418
- **RoHS/Green Compliant [6/6]**



APPLICATIONS

Model 636 is ideal for applications; such as digital video, networking equipment, broadband access, Ethernet/Gigabit Ethernet, microprocessors/DSP/FPGA, storage area networks, computers and peripherals, cameras and other portable devices to name a few.

ORDERING INFORMATION

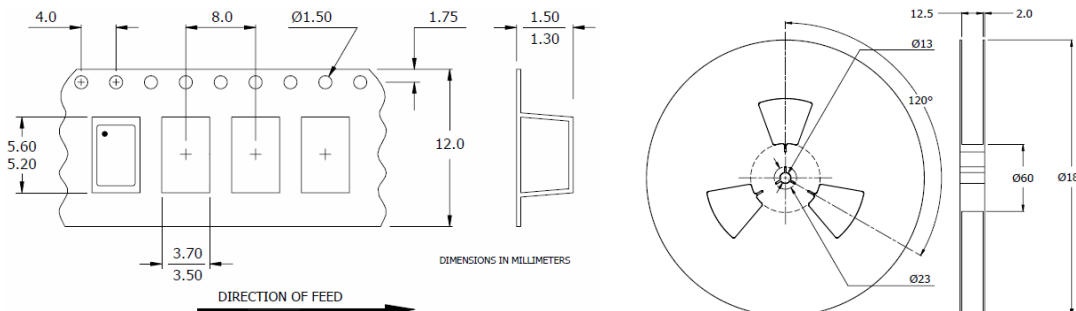


1] Consult factory for 6I Stability/Temperature availability.
 2] -40°C to +85°C Only.
 3] Frequency is recorded with three leading significant digits before the 'M' and 5 significant digits after the 'M' (including zeros).
 [Ex. 3.579545 MHz, code as 003M57954; 14.31818 MHz, code as 014M31818; 125 MHz, code as 125M00000]

**Not all performance combinations and frequencies may be available.
 Contact your local CTS Representative or CTS Customer Service for availability.**

PACKAGING INFORMATION [Reference]

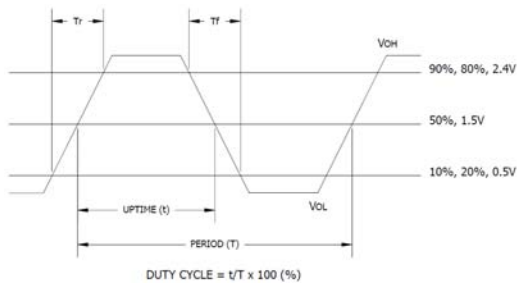
Factory may package reels in quantities of 1k pcs. or 3k pcs. Reel size is 180mm. **12mm tape width.**



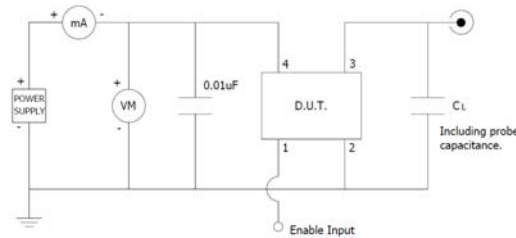
ELECTRICAL CHARACTERISTICS

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
ELECTRICAL PARAMETERS	Enable Function						
	Enable Input Voltage	V_{IH}	Pin 1 Logic '1', Output Enabled	1.26	-	-	V
	Model 636M		Pin 1 Logic '1', Output Enabled	1.75	-	-	
	Model 636N		Pin 1 Logic '1', Output Enabled	2.0	-	-	
	Model 636L		Pin 1 Logic '1', Output Enabled	4.0	-	-	
	Model 636S	Pin 1 Logic '1', Output Enabled					
	Disable Input Voltage	V_{IL}	Pin 1 Logic '0', Output Disabled	-	-	0.3	
Model 636M,636N,636L	Pin 1 Logic '0', Output Disabled		-	-	0.8		
Enable Time (M,N,L,S)	T_{PLZ}	Pin 1 Logic '1'	-	-	10	ms	
Standby Current	I_{ST}	Pin 1 Logic '0', Output Disabled	-	-	10	μA	

LVC MOS OUTPUT WAVEFORM



TEST CIRCUIT, CMOS LOAD

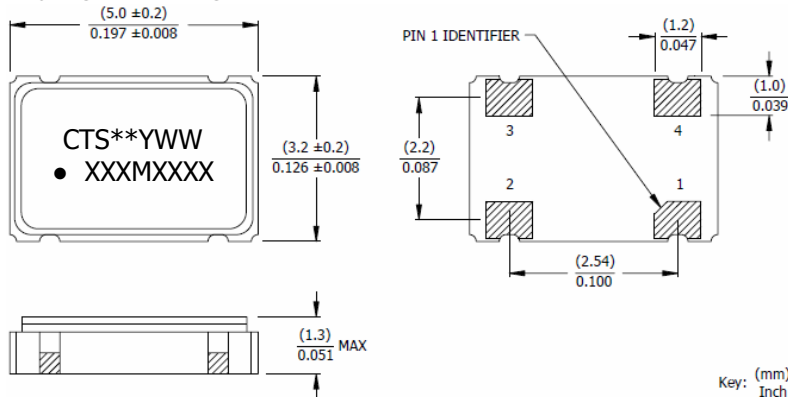


ENABLE TRUTH TABLE

PIN 1	PIN 3
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

MECHANICAL SPECIFICATIONS

PACKAGE DRAWING



MARKING INFORMATION

- ** - Manufacturing Site Code.
- YWW - Date code, Y - year, WW - week.
- XXXMXXXX - Frequency is marked with only leading significant digits before the 'M' and 4 digits after the 'M' [including zeros].
Ex. XXXMXXXX [62M5000]
XXXMXXXX [155M5200]

NOTES

- Termination pads [e4]. Barrier-plating is nickel [Ni] with gold [Au] flash plate.
- Reflow conditions per JEDEC J-STD-020, 260°C maximum, 20 seconds.
- MSL = 1.

D.U.T. PIN ASSIGNMENTS

PIN	SYMBOL	DESCRIPTION
1	EOH	Enable
2	GND	Circuit & Package Ground
3	Output	RF Output
4	V_{CC}	Supply Voltage

SUGGESTED SOLDER PAD GEOMETRY

C_{BYPASS} should be $\geq 0.01 \mu F$.

